Positive flatband voltage shift in phosphorus doped SiO_2/N-type 4H-SiC MOS capacitors under High Field Electron Injection

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Abstract. The effect of phosphorus inclusion on different bias stress at high electric field on phosphorus doped SiO_2 is investigated by electrical measurements of SiC MOS capacitors. 1 MHz $C-V$ measurements with (1) different bias hold time (up to 999 s at room and high temperature of 250°C), (2) different applied gate voltage (± 10, 20 and 30 V without stress time) and (3) different bias hold time at high voltage (± 30 V) were taken to observe the evolution of flatband voltage, effective oxide charge density and interface state density. In this investigation, the characteristics were measured in both sweep directions and compared to those obtained from undoped SiO_2 samples. At 250°C, the flatband voltage of phosphorus-doped SiO_2 samples shows a significant shift to the positive with increasing bias hold time. Similar trends are observed with the characteristics obtained at room temperature, but the shifts are less significant. Both undoped and phosphorus-doped samples show positive flatband shift when a higher bias was applied for longer hold times, but the latter demonstrated more significant changes. We conclude that the phosphorus ions increase the instability of the electrical characteristics related to the generation of mobile charges in the SiO_2, resulting in the injection of electrons from the semiconductor to the oxide. Therefore, the accumulated negative charge in phosphorus-doped SiO_2 resulting from the injection of electrons, which is enhanced by the mobile charge, is responsible for the enhanced positive shift in $C-V$ and $I-V$ characteristics.

Keywords: SiC, SiC/SiO_2 interface, interface states, MOS capacitors
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1. Introduction

Silicon carbide (SiC) is recognised as being a material of choice for high power, high temperature electronic sensors and circuits because of the superlative material properties, including the high critical breakdown field and wide bandgap [1]. However, SiC MOSFETs suffer from low channel mobility, which is determined by the high density of interface states (D_{IT}) present at the silicon carbide-silicon dioxide (SiC/SiO_2) interface under low gate bias [2, 3]. Significant research has already been undertaken to understand the origins of the interface states, so D_{IT} can be characterised and minimised to enhance the channel mobility. In contrast to silicon technology, hydrogen annealing has not been shown to reduce D_{IT} in SiC devices, and current research suggests either the growth of extremely thin oxide layers grown at very high temperatures [4] or nitridation (nitrous oxide annealing) [5] results in an enhancement in carrier mobility, related to the reduction in D_{IT} [6]. Additionally, the high concentration of trap states at the SiC/SiO_2 interface is linked to the bias temperature instability observed in SiC MOSFETs owing to thermal detrapping of electrons at high temperatures [7, 8, 9].

Incorporating sodium into the gate oxide has been shown to dramatically increase the field effect mobility of SiC MOSFETs by reducing the surface electric field [10, 11]. Unfortunately, the device is unstable in terms of threshold voltage (V_{TH}) when operating at high temperatures due to the presence of mobile charges in the oxide. The mobile charge densities are in the range of 10^{11} to 10^{13} cm^{-2}, which causes significant hysteresis in the $C-V$ characteristics, resulting in the flatband/threshold voltage instability, especially at high temperatures [12]. The presence of carbon in 4H-SiC results in a more complicated oxidation chemistry than that of silicon. For example, the oxidation of 4H-SiC is very slow [13] in comparison to silicon, and the generation of defects in the oxide and at the interface are inevitable [14].

Minimising SiC oxidation reduces the carbon impurity concentration at the interface, so field effect mobility could be increased by forming an ultra-thin SiO_2 interfacial layer between SiC and subsequent layers with a high dielectric constant (κ). The MOSFET comprising of a $SiC/SiO_2/Al_2O_3$ gate stack has successfully increased the field effect mobility up to 300 $cm^2V^{-1}s^{-1}$ [15]. However, V_{TH} typically reduces, becoming negative as the peak mobility increases. Alternative high-κ materials including La_2O_3 [16, 17], HfO_2 [18, 19] and Si_3N_4 [20], have also been reported as gate dielectrics.

Post oxide annealing (POA) [21, 22] has been confirmed to reduce the interface state density and hence increase the channel mobility in SiC MOSFETs. An effective POA of a SiO_2 gate dielectric is by incorporating phosphorus at the interface, which has been found to reduce D_{IT} near the conduction band [12]. This process can enhance the mobility resulting in values up to 89 $cm^2V^{-1}s^{-1}$ [23]; however, the long term stability of the flatband voltage (V_{FB}) in phosphorus doped MOS capacitors at high temperatures is still unresolved. The incorporation of phosphorus into SiO_2 changes the gate dielectric into phospho-silicate glass (PSG). In Si technology, a very thin PSG film has been used between the metal gate and SiO_2 layer to reduce the effect of mobile charge (Na^+

ion getter), stabilising the device characteristics. The improvement in charge stability and breakdown voltage of phosphorus doped SiO_2/Si MOS devices can be realised by a modification technique reported by Andreev, et al [24]. Using this technique, the characteristics of Si MOS devices are modified by electron injection at high electric field.

PSG is commonly used in the manufacture of semiconductor devices. A number of extensive studies have been published on the defect structure of the bulk material [24, 25, 26]. However, relatively little is known about the trapping characteristics of phosphorus-doped 4H-SiC/SiO_2 MOS capacitors [12]. The instability of the flatband voltage in phosphorus incorporated 4H-SiC MOS capacitors is due to the high concentration of defects at the interface and is a major concern in the bulk oxide, even at room temperature. This affects the device characteristics when measured under different gate bias conditions and results in variation of the extracted flatband voltage shift and threshold voltage shift [27]. It has been suggested that the origin of the flatband shift is due to the charge injection from the SiC substrate into the oxide [28]. Recently, mobile charge has been detected by triangular voltage sweep (TVS) measurements and this has been identified as the cause of the instability of SiC MOS devices at elevated temperatures [29]. Nevertheless, the intrinsic mobile charge in the oxidised SiC MOS capacitors can be reduced or increased by means of the post-oxide annealing treatment [28].

In this paper, a systematic investigation into the stability of phosphorus doped 4H-SiC/SiO_2 devices has been performed in MOS capacitors fabricated in a commercial process, through observations of the effects of high electric fields and bias time on the device characteristics. In particular, the flatband voltage, effective oxide charge density, interface state density and electron conduction mechanism have been explored at room and elevated temperatures, with direct comparisons made to a sample with a conventional thermal oxide gate dielectric. Understanding the origin of the flatband voltage shift in phosphorus doped SiO_2 devices is vital for the continued development of commercial 4H-SiC MOS devices.

2. Experimental

Two 100 mm, Si-face, 4°-off axis, 4H-SiC n^+ wafers with a 4 μm thick epitaxial layer doped with nitrogen at a concentration of 1×10^{17} cm^{-3} were used to fabricate MOS capacitors. Oxide films on both samples were fabricated by thermal oxidation, followed by post oxidation annealing. Then, a nitride cap was deposited to give an effective oxide thickness of 33 nm. For the phosphorus-doped SiO_2 device, subsequently referred to as "P-doped sample", one extra step was added to produce PSG oxide where the gate dielectric was annealed in a phosphorus rich environment (planar source of phosphorus pentoxide, P_2O_5) prior to metallisation. After aluminium gate deposition, both samples were treated with a conventional post metallisation annealing (PMA) to minimise the effects of high temperature measurements on the characteristics [30]. The fabrication

processes were designed to be compatible with a commercial CMOS process as described previously [31]. NMOS capacitors with photolithographically defined areas of 1.12×10^5 μm^2 were characterised using a Keithley 4200 semiconductor parameter analyser.

A range of gate bias conditions and bias stress times have been applied to observe the characteristics of the P-doped sample. The capacitors were held with different bias stress times (0 s to 999 s). Bidirectional 1 MHz $C-V$ measurements from accumulation (V_g = 10 V) to deep depletion (V_g = -10 V) were performed at room temperature and at 250°C. Furthermore, the same bidirectional measurements were repeated at room temperature, but with different starting gate voltages of 10, 20 and 30 V, and -10, -20 and -30 V for reverse and forward sweeps, respectively. Finally, the capacitors were held with different stress times at high bias, -30 V for forward sweep and 30 V for reverse sweep. The effects of bias voltage and stress time on the phosphorus doped SiO_2 devices were investigated from the changes in flatband voltage (ΔV_{FB}), with respect to data from the first measurement, effective oxide charge density (N_{EFF}) and interface state density (D_{IT}). Undoped SiO_2 MOS capacitor samples, subsequently referred to as "undoped samples," were used as a comparison. Fresh samples were used for each measurement to prevent the influence of charge accumulation in traps disturbing the data.

3. Results

Figure 1 shows the capacitance-voltage ($C-V$) characteristics for the undoped and P-doped samples for different gate bias stress times. The figure insets show the variation of the capacitance at the initial flatband voltage as a function of gate bias stress time. From this data, the flatband voltage and effective oxide charge are extracted, as shown in figure 2.

Figure 2 shows the flatband voltage V_{FB} and effective oxide charge density N_{EFF} as a function of gate bias stress time for typical samples from each set. These were extracted from the data based on an Al work function ϕ_M of 4.1 eV, SiC electron affinity χ_s of 3.1 eV [32], band gap E_{BG} of 3.26 eV, permittivity of SiC ε_s of $9.7\varepsilon_0$ with ε_0 being the vacuum permittivity, and intrinsic carrier concentration n_i of 10^{-7} cm^{-3} at room temperature [33]. V_{FB} was then determined from the C-V curves using the flatband capacitance $C_{FB} = C_{OX}(\varepsilon_s A/L_D)/(C_{OX} + (\varepsilon_s A/L_D))$, where C_{OX} is the oxide capacitance, A the effective gate area and L_D the extrinsic Debye length of $\sqrt{\varepsilon_s kT/(e^2 N_D)}$, with e being the electronic charge. N_{EFF} was subsequently calculated from $N_{EFF} = C_{OX}(\phi_{MS} - V_{FB})/(eA)$, where ϕ_{MS} is the difference in work function between the metal contact and semiconductor [12].

The plots show the effect of sweep direction from a starting bias of ± 10 V measured at room temperature (figures 2 (a) and (b)) and at 250°C (figures 2 (c) and (d)). Under forward sweep, the shift in flatband voltage (ΔV_{FB}) and effective oxide charge density (N_{EFF}) for the undoped sample are negligible (less than 0.3 V) at both room temperature and 250°C for the stress times investigated in this work. However,

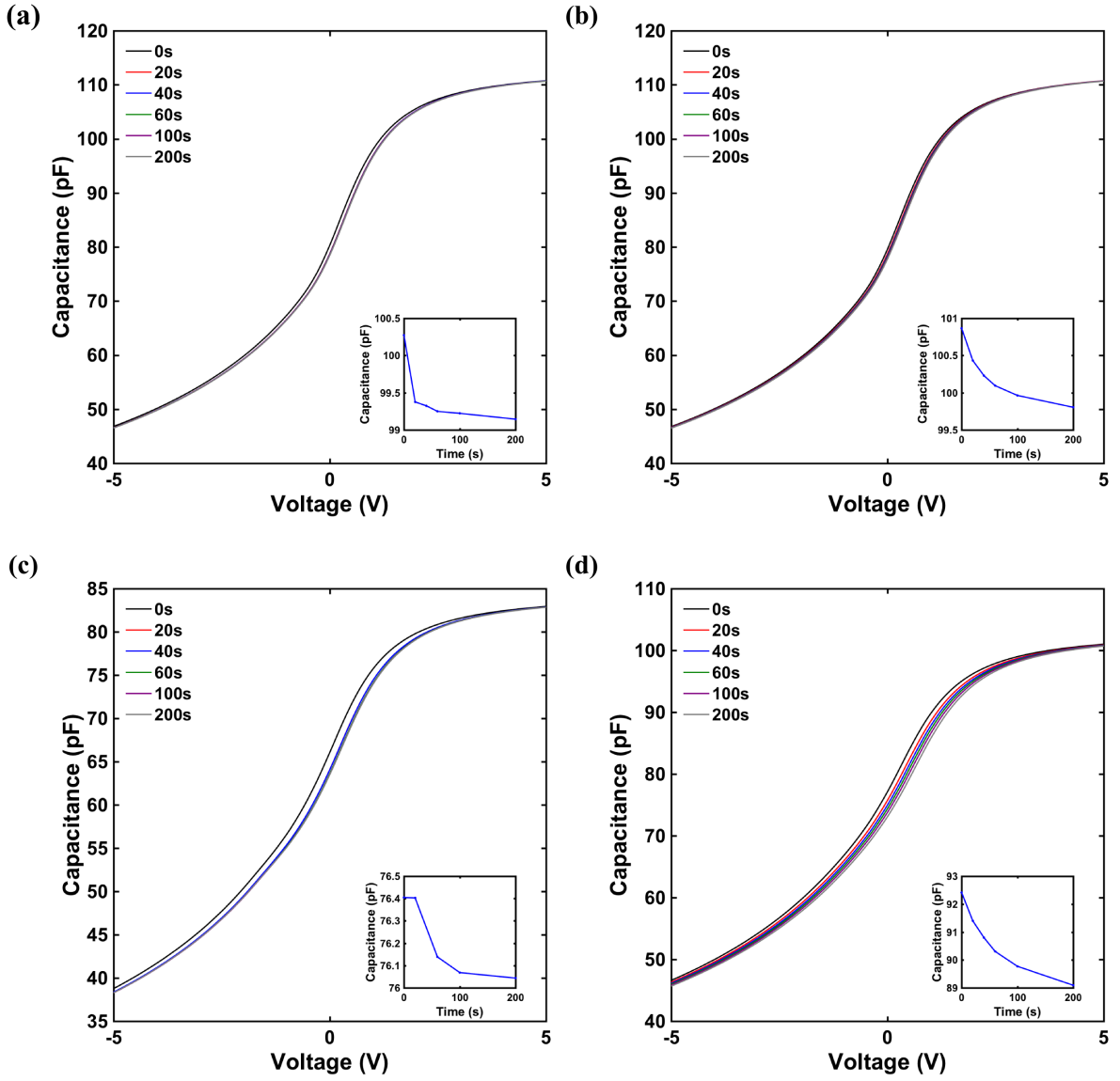

Figure 1: C-V measurements at different gate stress times for **(a)** undoped sample under forward sweep, **(b)** undoped sample under reverse sweep, **(c)** P-doped sample under forward sweep and **(d)** P-doped sample under reverse sweep.

significant changes in flatband voltage (up to 0.7 V for a hold time of 999 s) and effective oxide charge (up to -7×10^{11} cm^{-2}) are observed for the P-doped sample under reverse sweep conditions at room temperature as the bias stress time is increased. The shifts for the P-doped sample for both ΔV_{FB} and ΔN_{EFF} become more apparent at 250°C under reverse sweep where the flatband voltages increase rapidly by 2 V for stress times between 0 and 200 s, before starting to saturate at approximately 2.5 V above the initial data set after 500 s. The same trends were observed at 250°C for the effective oxide charge as the bias stress time increases. These data are consistent with the instability of phosphorus-doped SiO_2 due to charge trapping at the interface and mobile charges

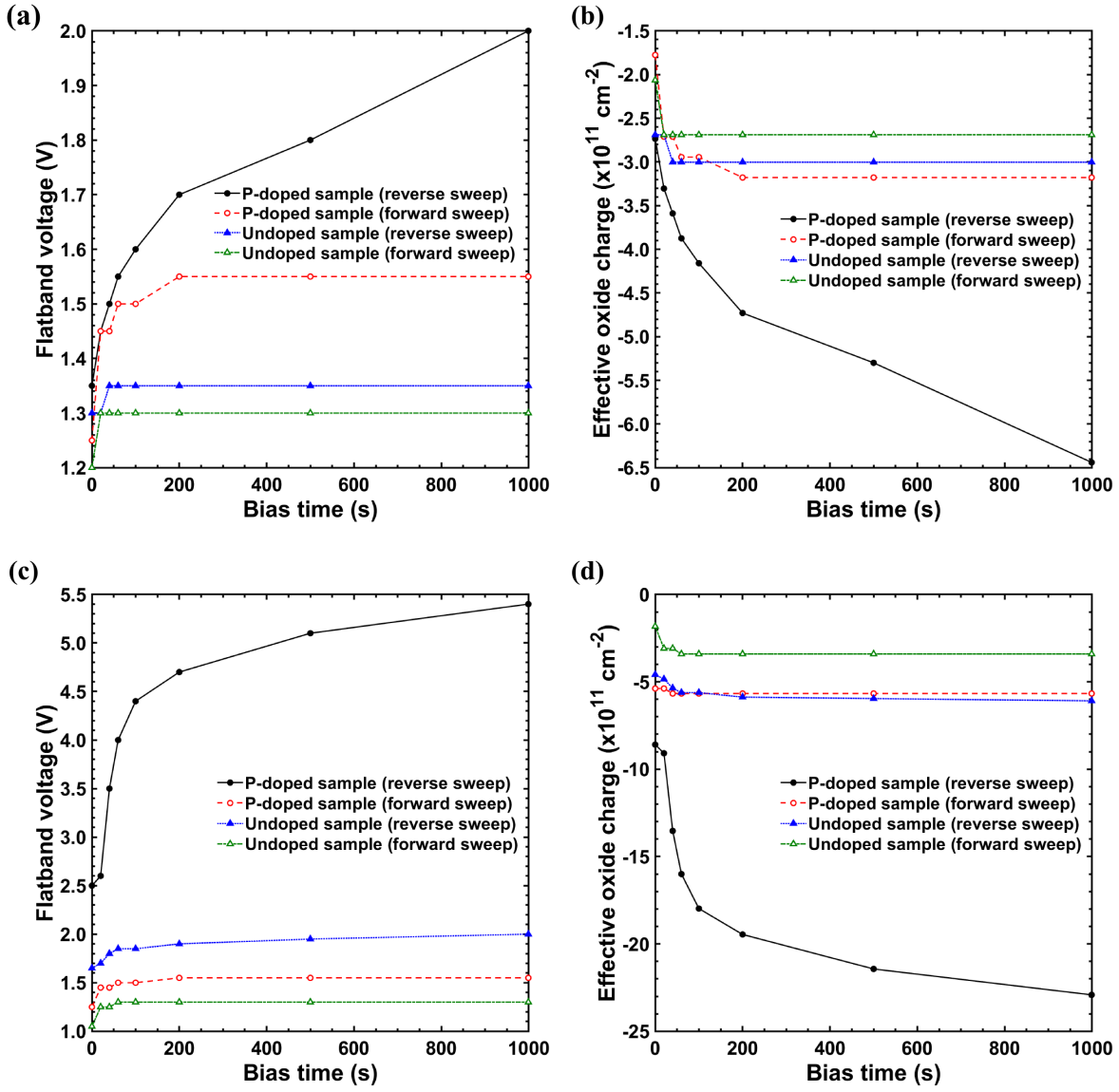

Figure 2: Flatband voltage (V_{FB}) and effective oxide charge density (N_{EFF}) under different gate bias stress times at the room temperature ((a) and (b) respectively) and 250°C ((c) and (d) respectively) extracted from 1 MHz $C-V$ curves. The samples are typical examples of the different gate annealing treatments.

in the oxide, which cause the electrons to be injected into the bulk oxide and results in the increasingly negative effective oxide charge [12].

As reported in the literature, the effective oxide charge in MOS capacitors can be modified by the injection of electrons into the gate dielectric, which typically occurs at high electric field [34, 35]. The probability of electron injection from the semiconductor to the gate dielectric or from the gate contact to the gate dielectric is increased at high temperatures because of potential barrier lowering and the number of electrons gaining sufficient energy to overcome the barrier height (so called hot electrons) [35].

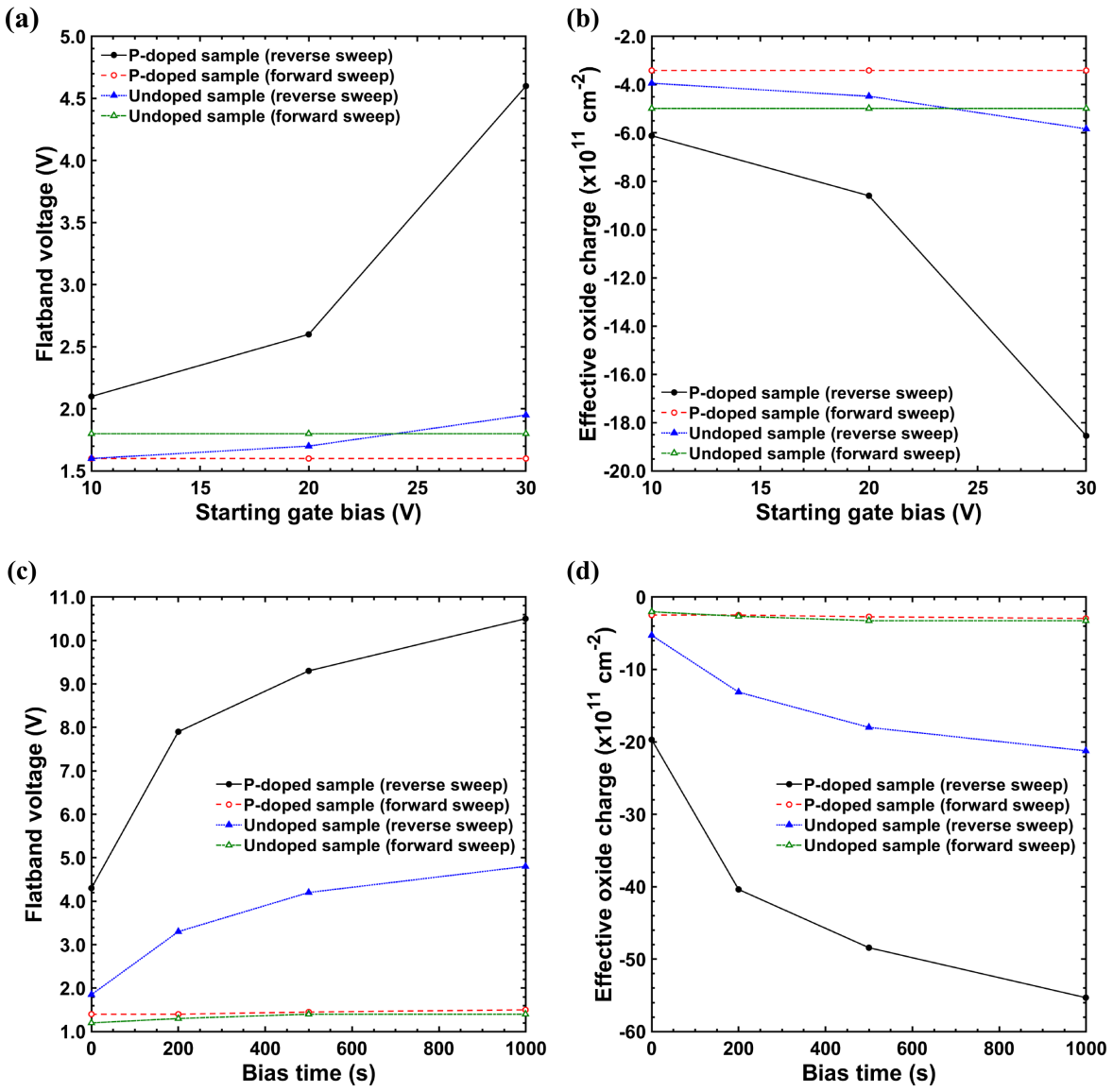

Figure 3: Flatband voltage (a) and effective oxide charge density (b) under reverse sweep at room temperature under different gate bias conditions. Flatband voltage (c) and effective oxide charge density (d) at high voltage (±30 V) with different bias stress time up to 999 s.

The consequence of this phenomenon includes increased leakage current due to the degradation of the gate dielectric via Fowler-Nordheim tunnelling [35]. In SiC, since the interface trap density is high in comparison to Si, the charge carriers can become trapped close to the interface, permanently changing the characteristic behaviour of the dielectric, resulting in instability of the device characteristics. For phosphorus-doped SiO_2, the carriers traverse the SiC/SiO_2 interface, which leads to accumulation of negative charge in the bulk of the phosphorus-doped gate dielectric, resulting in the observed positive shift of the flatband voltage.

In order to investigate the stability and the effect of electron injection at different

electric fields on the flatband voltage and effective oxide charge, 1 MHz $C-V$ measurements with starting gate bias conditions of -10, -20 and -30 V for forward sweep and 10, 20 and 30 V for reverse sweep were performed. Figures 3(a) and (b) show the effect of starting voltage on the parameters extracted from the $C-V$ characteristics without bias stress time on the stability of flatband voltage and effective oxide charge, respectively. As described previously, the changes in both flatband voltage, and effective oxide charge are less significant under a forward sweep for both samples. Under reverse sweep conditions, the flatband voltage and effective oxide charge in the phosphorus doped samples increase with starting voltage. Both the flatband voltage shift and change in effective oxide charge are greater (up to 2 V and -2 $\times$ 10^{12} cm^{-2}, respectively) in comparison to the thermally grown oxide for a starting bias of 30 V.

Figures 3 (c) and (d) show the changes in flatband voltage and effective oxide charge as a function of bias stress time when the device was held at 30 V (forward sweep) and -30 V (reverse sweep), respectively. The changes in flatband voltage and effective oxide charge are negligible under forward sweep conditions. During the reverse sweep, the shifts in flatband voltage and effective oxide charge increase with bias stress time for both samples and the rate of change reduces as the stress time is increased, indicating that the charge trapping effect is apparent under the reverse sweep condition.

For both samples the positive shifts in V_{FB} occur at higher voltages when longer bias stress times were applied. As can be seen in figures 3 (c) and (d), the shift in the flatband voltage and effective oxide charge increased, following a $t^{1/2}$ relation with bias stress time, suggesting there is a limit to the charge density that can be injected prior to oxide breakdown. These results are in good agreement with those reported previously for phosphorus doped SiO_2/Si MOS capacitors [24, 34]. Andreev, *et al.* observed that the injected charge density depends on the thickness of the phosphorus-doped oxide with the accumulated negative charge density increasing with increasing phosphorus-doped SiO_2 film thickness [34]. Reports in literature have also shown that the stability of phosphorus-passivated 4H-SiC MOSFETs can be improved by reducing the thickness of the interfacial PSG gate dielectric layer [36]. In n-type devices, the density of interfacial acceptors is considerably higher than the donor concentration. An increase in the PSG film thickness is unacceptable for thin gate dielectrics, as this leads to excess doping of the SiO_2 film with phosphorus and as a consequence, leads to deterioration in the charge stability of the bulk oxide and at the interface. It has also been reported that an increase in the phosphorus concentration in the PSG film to more than 1.5% may cause polarization and a decrease in the charge stability of the gate dielectric [24].

To study the origin of the changes in flatband voltage and effective oxide charge, the interface state density was extracted using the Terman method [12] as a function of bias stress time, as shown in figure 4. Both samples exhibit an increase in interface state density when the oxide is subjected to a bias ($V_g = 30$ V) for 200 s. The interface state density does not change significantly for bias stress times longer than 200 s suggesting that all the available states have been filled. The observed increase in D_{IT} for the PSG sample with bias stress time (P-doped sample) in comparison to the undoped SiO_2

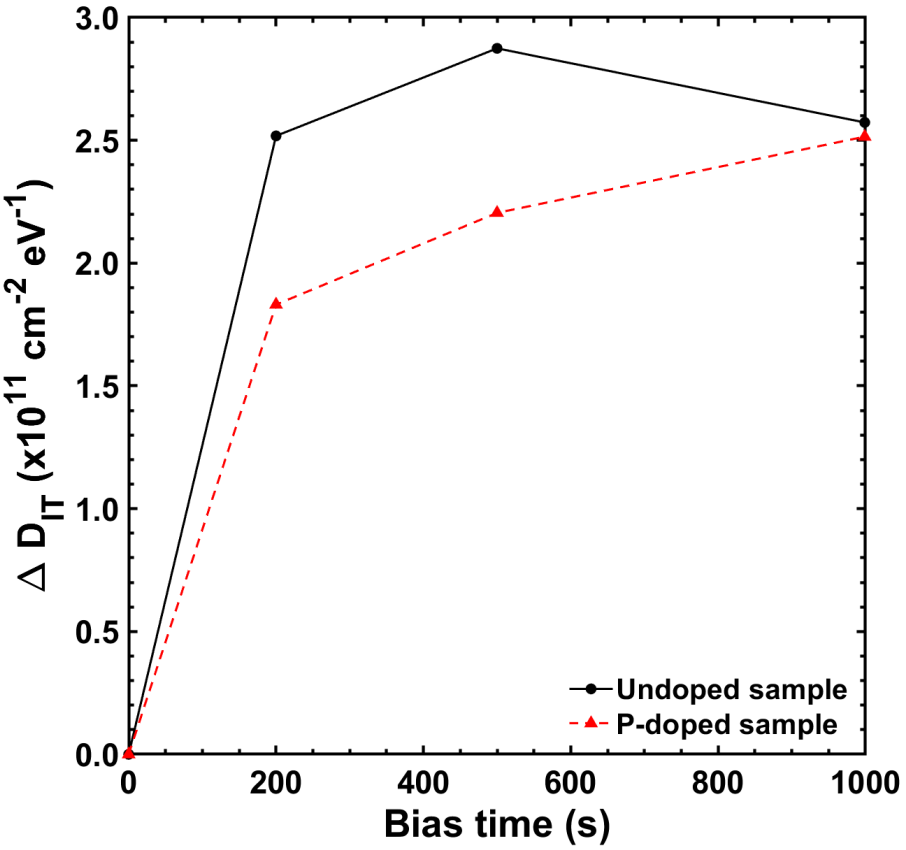

Figure 4: The changes of D_{IT} as a function bias stress time for undoped and P-doped samples under reverse sweep measured from V_g= -30 V at room temperature.

(undoped sample) is one possible origin of the larger positive flatband shift.

The Weibull distributions of the accumulated field strength ($E_{OX}.t_{BD}$) of the gate dielectric are shown in figure 5. The accumulated field strength used in the Weibull plot describes the energy in the oxide at the point of failure for a constant current, normalized to the sample thickness. This removes the influence of the different oxide thickness resulting from the phosphorous incorporation. Capacitors with and without phosphorus treatment display two distinct distributions. Firstly, the Weibull distribution slopes for the phosphorus doped capacitors are steeper than those for the undoped devices. The deviation of the statistical failure rate between 0 to -3 in the undoped samples indicates a lower uniformity in the distribution. Secondly, P-doped sample shows a highly repeatable distribution and this allows a higher level of repeatability during fabrication. In fact, a noticeably higher breakdown electric field for phosphorus passivated MOS capacitors was reported when compared to conventional annealing in nitric oxide [36].

Under constant current stress conditions, the applied current is constant but the electric field increases with hold time. For each distribution, Weibull slopes (β) can be extracted and can be used as a metric for oxide quality, giving β=1.38 and β=6.47

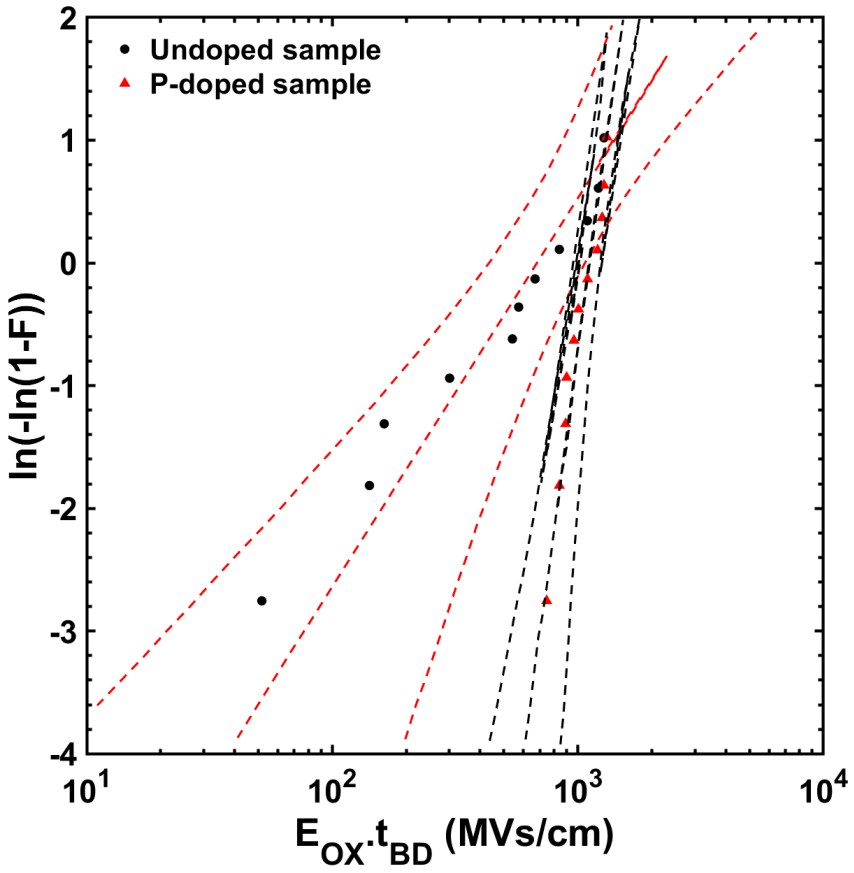

Figure 5: Weibull distribution of constant current for all MOS samples in oxide field strength (E_{OX}) and elapsed breakdown time (t_{BD}). The dashed lines represent 95% confidence intervals.

for undoped and P-doped samples, respectively. Normally, the distribution represents the intrinsic reliability of the oxide, therefore, theoretical β values for oxide films with a thickness between 30 and 110 nm are typically in the range of β=7 on Si/SiO_2 [37]. The significant increase in the Weibull slope for the P-doped sample in comparison to the undoped sample, along with the tighter confidence bands, indicates an increase in reliability. The relatively large β value for P-doped sample suggests the oxide breakdown distribution is more intrinsic than in the undoped SiO_2. The degradation and breakdown of the gate dielectrics are related to the probability of charge trapping which results from the increased interface state density under high current stress [37], and hence, a reduced time-dependent dielectric breakdown.

Quantum mechanical tunneling describes the movement of carriers through a classically forbidden energy state. Figure 6 shows the current characteristics as a function of electric field for both samples measured at room temperature and 100°C. For the undoped SiO_2 samples, the $I-V$ curves are consistent on the first, second and third measurements. In contrast the phosphorus-doped SiO_2 are shifted to the positive every time the measurement is repeated. The accumulation of negative charge

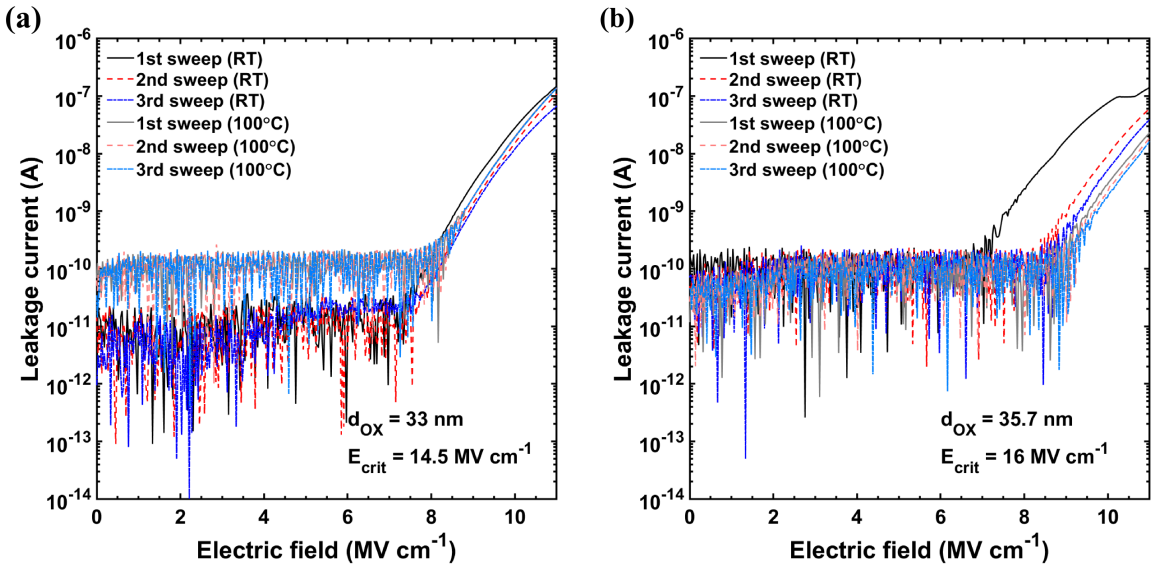

Figure 6: I-V characteristics of (a) undoped sample and (b) P-doped sample at room temperature and 100°C.

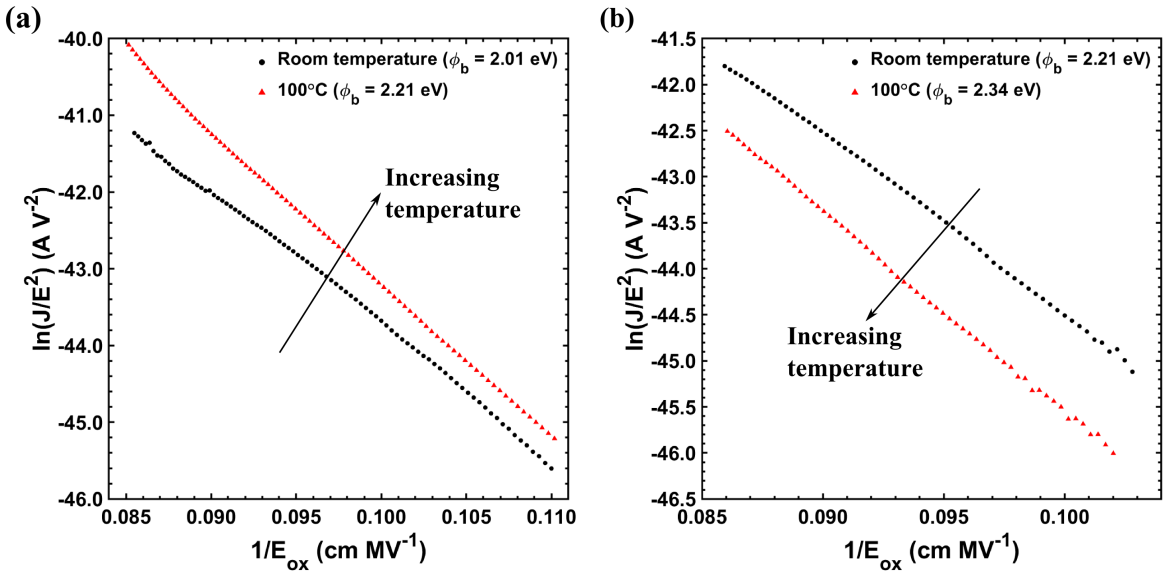

Figure 7: FN plots of (a) undoped and (b) P-doped samples at room temperature and 100°C.

in the gate dielectric shifts the $I-V$ curves in a positive direction and increases the breakdown voltage by changing the charge state of the defects in the gate dielectric [34]. This effect can be explained by reducing the concentration of uncharged defects through the accumulation of a negative charge in the gate dielectric by increasing the amount of charge injected into the dielectric. As a result, the potential barrier increases, thus increasing the breakdown voltage.

Fowler-Nordheim (FN) plots are a useful method to determine the relation between the strength of electric field (E) and barrier height (ϕ_b), using $J/E^2 = A\exp(-B/E)$,

where J is the current density, and A and B are the pre-exponential constant and slope, respectively, given by $A = e^3 m_0/(16\pi^2 \hbar m_{ox} \phi_b)$ and $B = 4(2m_{ox})^{1/2}\phi_b^{3/2}/(e\hbar)$, where m_0 is the free electron mass, m_{ox} the electron mass in the oxide of $0.42m_0$, and $\hbar$ is Planck's constant [38, 39]. Figure 7 shows FN-plots ($(\ln(J/E^2)$ as a function of inverse electric field $(1/E)$) for both samples measured at room temperature and 100°C. The barrier height, ϕ_b, for both samples are extracted from the FN slopes, and found to be 2.01 and 2.21 eV for undoped sample at room temperature and 100°C, respectively, and 2.21 and 2.34 eV for P-doped sample. Due to the quantization effect in the accumulation layer and image force lowering, the values of ϕ_b extracted are expected to be approximately 0.3 eV lower than those obtained by internal photoemission experiments of 2.77 eV, implying the presence of defect states in the upper half of the bandgap, closer to the conduction band edge [40]. The interface state density which enhances the electron trapping and oxide degradation not only affects the channel mobility, but also influences the barrier height by acting as a primary source for FN tunneling [41].

As the temperature was increased to 100°C, $\ln(J/E^2)$ increased for the undoped sample, but decreased for the P-doped sample. The rate at which the leakage current increases with electric field determines the breakdown voltage, i.e. the faster the leakage current increases with field, the smaller the breakdown voltage. Therefore, the increased leakage current in the undoped sample at 100°C indicates a lower breakdown voltage, whilst the decreased leakage current in the P-doped sample suggests an increase in breakdown voltage with temperature. The accumulation of negative charge in the PSG film, due to phosphorus atoms enhancing electron injection into the gate dielectric [12, 34, 42], leads to an increase in the energy barrier [39] at the injection interface boundary, which increases the breakdown voltage of the gate dielectric.

4. Discussion

Metal contamination such as sodium and potassium are considered to be the origin of mobile ions in metal-oxide-semiconductor devices. In this study, contamination is unlikely to be the cause of the difference in mobile ions due to the fabrication of both devices being the same, with the exception of phosphorus doping of the SiO_2 in the P-doped sample. The results show that the flatband voltage of phosphorus doped SiO_2 is shifted to the positive under reverse sweep as the bias stress time increases at room temperature and the changes are more pronounced at 250°C. Enhanced shifts to the positive are observed when high starting voltages are used with the C-V measurements. This phenomenon is more noticeable when high voltage and longer bias stress times are used. Under forward sweep conditions, the flatband voltages are stable and result in a shift that is negligible in comparison to the flatband voltage shift under reverse bias.

The possible origin for the positive flatband voltage shifts can be explained by the enhanced electron injection linked to the existence of traps at the interface resulting in an increased mobile charge density. Positive shifts occur when the acceptor-like deep interface states are filled with electrons under strong accumulation conditions.

As previously reported in [12], the mobile charge density in phosphorus doped SiO_2 is high in comparison to thermally grown oxide, due to the gettering effect that removes undesirable impurities, increasing the quantity of mobile charge [43]. The mobile charge density has been determined from the bias temperature instability, where the mobile ions are able to move at high temperatures. In this experiment, the data shows that the ions are highly mobile at room temperature if high electric fields are applied for long periods.

Figure 8 shows a schematic of electron injection from the semiconductor into the oxide with assistance from mobile ions, which are likely to result in the observed ΔV_{FB}. Positively charged ions in the phosphorus doped SiO_2 capture accumulated electrons from the surface of the semiconductor [28]. When a high electric field was applied to the gate, electrons were injected into the dielectric, resulting in a negatively charged oxide, so a shift in flatband voltage was observed [24]. At high temperature and under a high electric field, the mobile charge in the oxide will move to the interface, or away from the interface depending on the polarity of applied bias.

Interface traps can be either acceptor-like or donor-like, with the donor-like trap

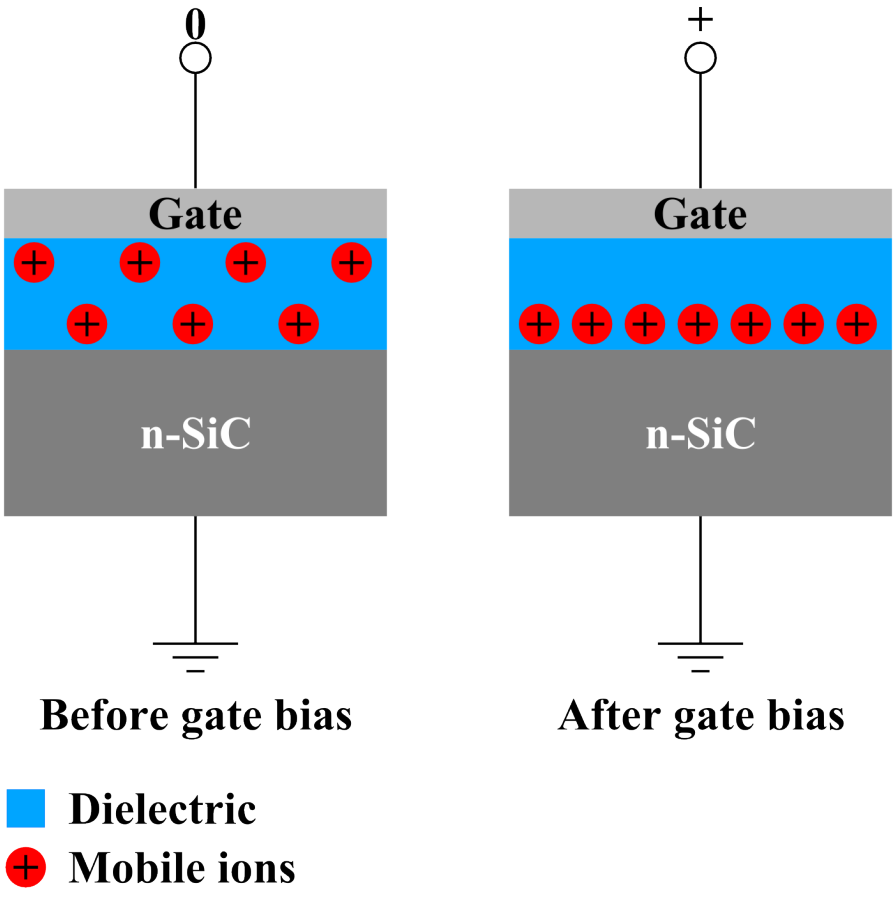

Figure 8: Mobile charges are moved to near the interface between the dielectric and SiC as the constant high voltages are applied with certain bias stress time.

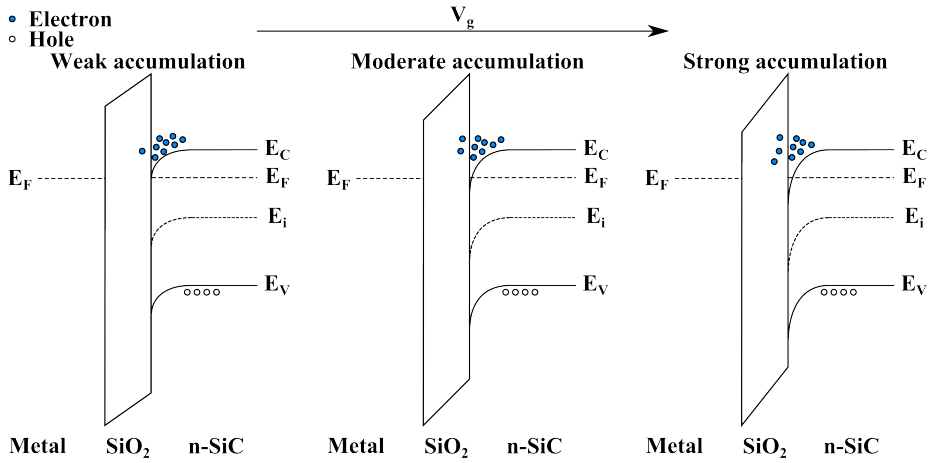

Figure 9: Electron injection from semiconductor into the oxide under reverse sweep at different voltage with different hold bias stress.

energy levels located in the lower half of the band-gap. Those trap levels are positively charged if they are empty and electrically neutral when occupied by an electron. The acceptor-like energy levels are located in the upper half of the band gap, and are electrically neutral if empty and negatively charged when occupied by an electron. Figure 9 illustrates the band diagram for an n-type MOS capacitor under positive bias (accumulation), where the majority of electrons are accumulated at the interface. Similarly, states in the upper half of the band gap become occupied and result in the oxide becoming negatively charged. The electrons are increasingly injected from the semiconductor into the oxide under high field conditions as band bending exposes the defects that lie close to the Fermi level. Injection of electrons (hot carriers) into the oxide occurs easily at the SiC/SiO_2 interface because the electric fields in SiC devices are much higher than in silicon and the barrier height at the SiC/SiO_2 interface is lower than the barrier height for Si/SiO_2 [41]. As the temperature increases, electron injection becomes more dominant [44] as the increased temperature results in the effective barrier height reducing and the thermal energy of electrons increasing. Thus electrons gain sufficient energy to overcome the barrier at the interface, so are injected into the dielectric. It has been reported that the injection of electrons into oxide generates interface states that are not only affecting the channel mobility but also influencing the barrier height for Fowler-Nordheim tunneling [39].

5. Conclusion

The incorporation of phosphorus in the oxide and at the SiO_2/SiC interface shifts the magnitude of flatband voltage and increases the effective oxide charge. The influence of phosphorus incorporation in the gate dielectric was investigated using $C-V$ measurements at voltages up to 30 V with bias hold times up to 999 s. In forward sweep, the flatband voltages and effective oxide charges are stable even at high voltage

and long bias stress time. However, in reverse sweep, the flatband voltage and effective oxide charges increase significantly especially at higher starting voltages and for longer bias stress times. This can be attributed to the capture of electrons at the interface during positive bias stress. The effect becomes more prominent when phosphorus atoms exist at the interface because of the gettering effect that increase the quantity of mobile charge in the oxide. The data also reveals that electron injection is more likely to occur in phosphorus doped SiO_2, due to the high density of mobile charge in the oxide and this leads to instability in $C-V$ characteristics, especially at high temperatures. The presence of phosphorus atoms in the oxide results in a greater concentration of mobile charges, which correlates to the enhanced flatband shift and the increase in effective oxide charge, when higher voltage and longer stress times are applied. The $I-V$ characteristics for both samples were compared and it was found that for the phosphorus doped samples, the breakdown electric field increased when the same measurements are repeated. The same mechanism of electron trapping and electron injection can be explained for the instability of phosphorus doped SiO_2 in 4H-SiC MOS capacitors.

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